3D-IC challenges: design with test (Part 1/2)

With numerous product announcements and technological advancements in the past 12 months, 3D-ICs using through-silicon vias (TSVs) have emerged as a proven, viable technology that offers compelling advantages in power, performance, form factor, and time-to-market.

By making it possible to stack analog, digital, logic, and memory dies at different process nodes, 3D-ICs offer what may be the best alternative to the skyrocketing costs of advanced process nodes.

There are multiple design challenges in 3D-IC silicon realization, as noted in a recent whitepaper and Chip Design Magazine article. However, design for test (DFT) is one of the most challenging areas. 3D-IC stacks will be deployed only if they are cost-effective, and they will be cost-effective only if they're testable and offer reasonably good yields.

While wire-bonded systems-in-package (SiPs) may have a few hundred interconnects, 3D-ICs may have thousands if not tens of thousands of interconnects. Even a single defective TSV can render an entire stack unusable. If individual TSVs have 99.9% yield, at least one defective TSV can be expected in a stack with 1,000 TSVs.

A sound test methodology for 3D-ICs is necessary in order for IC designers to have the confidence to design them. Designers will not start 3D designs without knowing how to make them fully testable. Likewise, test equipment manufacturers and assembly houses cannot plan a production test environment without knowing which failure mechanisms to look for, how to cost-effectively assure known-good die (KGD) prior to stacking, and how thoroughly test stacks during the assembly process, and how to best perform exhaustive final tests.

Some obvious questions around 3D-IC DFT are: Who tests what portion of a 3D stack, and when? Are there new fault types associated with TSVs and micro-bumps? How can testers access TSVs and micro-bumps, since they are too small or today's probe technology? Will transistor behavior change due to the wafer thinning process? Is it possible to control and observe individual dies, even though the only access to test signals is usually on the bottom die in the stack?

Fortunately, solutions are starting to emerge. A number of papers and tutorials at recent conferences and workshops have addressed challenges and potential solutions for 3D-IC test.

Innovation is ongoing both in design for test (DFT) and in tester and probe card technology.

This article provides a general overview of 3D-IC test challenges, and describes a DFT architecture developed at imec research institute in cooperation with Cadence Design Systems. The architecture enables the modular testing of dies and TSV-based interconnects by using die-level wrappers that isolate the individual dies from the stack. A subsequent article will focus on needed improvements and technical progress in tester and probe technology.

3D-IC test challenges – Test flows

According to Erik Jan Marinissen, principal scientist at imec, 3D-IC test challenges can be understood in terms of test flows (what to test when), test content (what test data is needed for likely defects), and test access (how to probe and access test signals).

A conventional 2D test flow is proven and straightforward. It involves wafer probe, and, after packaging, final test. In the 3D world a disaggregated flow is much more likely. The individual dies are likely to come from different wafer fabs, and there are many questions about what should be tested when. Should dies be tested before stacking, and do they need KGD final-test quality, which includes at-speed testing and burn-in? Should interconnects be re-tested every time a new die is added to the stack, or not until the entire stack is assembled? What will the final test include and who will do it?

At one extreme, it is possible to spend too much time and money on continual re-testing. At another extreme, not testing enough may result in a "penny wise and pound foolish" approach that results in low yields, Marinissen said. He noted that careful cost and yield modeling is needed to determine what steps the test flow should include for any given 3D-IC.

Pre-bond testing is done on the original or thinned-down wafer before stacking. It can be challenging for any die that will not be the bottom die in the stack. These "upper" dies receive all functional signals (power, clocks, control, data)
through TSV interconnects, which are too small for current probe technology to handle. One workaround is for the IC designer to bring test signals out to larger, dedicated pre-bond test pads.

Unless yields for the individual dies are very high, pre-bond testing is probably cost-effective. If individual dies are likely to have only a 90% yield, and four dies are placed in a 3D stack, the yield of the completed stacks will only average around 66%. It is less expensive to find a defective die at the pre-bond level than during post-bond testing.

Post-bond testing is done on a partial or complete stack. It assesses the quality of TSV-based interconnects between stacked dies, and checks for additional defects that may have occurred due to stacking. Probe access is available only on the external I/Os of the stack, which are typically located on the bottom die only. Fortunately, the bottom die external I/Os lead to conventional wire-bond pads or flip-chip bonds that do not provide major test access challenges. However, the DFT architecture needs to propagate test data from the external I/Os up and down through the stack.

Post-packaging (or final) testing serves as the final check that determines the outgoing product quality to the customer. The designer should be able to test any die and TSV-based interconnect layer in the stack. Test access will not require wafer probing, but will instead be based on sockets.

Ultimately, board-level interconnect test and board-level hardware/software debug will also be needed. For board test, the 3D-IC should be as transparent as possible to the board designer, and board testers should only need to access the boundary scan interface of the stack.

### 3D-IC test challenges – Test content

All manufacturing defects that can occur in conventional 2D chips are relevant when these chips are in 3D stacks, including stuck-at, transition, delay, and IDDQ faults. However, the designer needs to provide new test content because there are new types of potential defects, particularly those due to added 3D processing steps and TSV-based interconnects.

One 3D processing step that can cause new defects is wafer thinning. TSV processing only allows limited heights and aspect ratios. If a TSV has a 5µm diameter and 1:10 aspect ratio, this would dictate a height of 50µm. To expose the TSVs, the wafer must be thinned to 50µm from an original thickness of 750µm. Wafer thinning may change transistor performance, degrade I-V characteristics, and cause yield losses.

Defects may also be due to thermal expansion and thermo-mechanical stress. Dies in the middle of a stack are especially prone to higher temperatures, and excessive heat can change the performance of devices or even lead to damage. Test itself can be a danger, as at-speed test may cause dies to heat up excessively. Designers must ensure adequate power to all dies in a stack, and avoid excessive noise or voltage drop.

TSV-based interconnects may introduce defects during fabrication (liners, barriers, plating) or interconnect bonding (oxidation, contamination, height variation, misalignment). Opens, shorts, and timing faults are possible. Imec and Cadence have worked together to develop an interconnect fault model and automatic test pattern generation (ATPG) capability to detect such defects.

### 3D-IC test challenges – Test access

Current probe technology cannot access TSVs or micro-bumps. TSVs typically have diameters around 5µm and a 10µm pitch, while micro-bumps may have diameters of 25 µm and a 40µm pitch. The minimum in-line pitch for today’s advanced wafer probe technology is well over 50µm. Further, probes may leave scrub marks or cause pad damage. The industry is working to improve probe technology, but in the meantime, the IC designer should plan on adding dedicated pads in the DFT architecture.

A modular 3D-IC test architecture, in modular testing, chip modules such as embedded cores are tested as standalone units. Modular system-on-chip testing also enables heterogeneous circuit structures, “divide and conquer” ATPG, and test reuse. Modular testing of 3D-ICs can provide these capabilities as well as easy yield monitoring, first-order fault diagnosis, and the ability to flexibly optimize the 3D-IC test flow.

A 3D-IC DFT architecture, originally created at imec, was further developed and refined in co-operation with Cadence. The architecture has been proposed as a standard test-access architecture through the IEEE P1838 3D Test Working Group, which represents EDA, IP, ATE, and semiconductor vendors. “In the end, we feel it needs to be an industry solution,” Marinissen said.

In this DFT architecture, wrappers provide isolation and boundary-scan access for the internal testing of individual dies as well as interconnect between dies. The architecture supports pre-bond, mid-bond, and post-bond testing. It allows and complements any test structures that may be used on the individual dies, such as scan or BIST. “The architecture provides a way to get test data from any of the chips in the stack without overly
consuming a lot of test signals,” said Brian Keller, senior architect at Cadence.

The architecture supports both IEEE 1500 (Embedded Core Test) and IEEE 1149.1 (JTAG) wrappers, but most of the initial work has focused on IEEE 1500. While the wrappers perform similar functions, there’s a difference. IEEE 1149.1 uses a single-bit instruction/data interface, two or three control inputs, and a Test Access Port (TAP) controller. IEEE 1500 also provides a single-bit serial interface but allows a scalable n-bit parallel data interface, along with six or seven control inputs.

The architecture also adds several 3D enhancements to test wrappers. One is called a "test elevator.” As previously stated, post-bond test access is typically available only from the bottom die in the stack. A test elevator is needed to pass test data to and from dies above the bottom die, using dedicated TSVs. A design with 1,000 functional TSVs may only require 20 or so of these special test TSVs. Another wrapper enhancement allows “test turns” that return the test signals within a die, rather than passing signals on to the next die. Enhancements also provide additional probe pads for pre-bond test, and add registers to provide a clean timing interface to output paths. A hierarchy of instruction control registers makes it possible to selectively test higher-level dies.

A 3D-IC DFT architecture will only succeed if it can be implemented in EDA tools. For this reason, Cadence and imec have collaborated to develop a wrapper generation flow using the Cadence Encounter RTL Compiler, and an innovative ATPG solution using interconnect fault modeling for TSVs and micro-bumps in Cadence Encounter Test. This interconnect ATPG is very efficient – a design with a million interconnects may require just tens of dedicated patterns. The solution uses what is called a “boundary skin” model that provides just enough information about the die to generate ATPG patterns.

Conclusion

3D-IC test is challenging, but it does not need to become a bottleneck. If design and manufacturing teams understand the challenges and work together, they can develop an appropriate test flow by doing cost modeling, adding test content for new 3D failure mechanisms, and using dedicated probe pads so long as probe technology cannot provide full access. A modular 3D-IC

DFT architecture, such as the one described here, can alleviate many test challenges while providing controllability and observability for individual dies and TSV interconnects. A standardized DFT architecture through IEEE P1838 will simplify a 3D-IC design, manufacturing and test flow supported by multiple industry providers.

To be continued in the November issue of 3D Packaging

Santa Bansal leads 3D-IC efforts among others for Applied Silicon Realization at Cadence Design Systems, Inc. She has more than 12 years of experience working with semiconductor leaders including both 2D and 3D IC design space. Prior to Cadence, Santa worked at Synopsys looking into the front end technologies. With hands on experience on front end for 8 years and moving to back end, Santa has a very good understanding of the evolution and challenges the industry has been going in terms of design requirements and is very passionate in driving this shift of the industry from 2D to 3D IC within Cadence and working with the ecosystem partners. Santa has Masters in Physics, Bachelors in EEE from Birla Institute of Technology and Science(BITS), Pilani and MBA from Santa Clara University.

Herb Ritter, chair of the GSA's 3D-IC Working Group and consultant for the GSA since 2008. He founded edaZaiz Consulting in the spring of 2002 to increase cooperation between EDA suppliers and semiconductor vendors. In this role Herb introduced many EDA tools, flows and methodologies to reduce IC design time for the semiconductor vendors and to lower power dissipation and unit cost for their products. Previously Herb worked for 5 years in business development roles at Barcelona Design, Synopsys and Viewlogic. The PrimeTime sign-off wave and the TSMC reference flow #1 are highlights of Herb's accomplishments at Synopsys. From 1980 to 1997 Herb worked in both business and technical roles at VLSI Technology and National Semiconductor to market ASIPs and ASSPs. Herb earned an MBA at San Jose State University and Master Degrees in Business and in Electrical Engineering at the University and at the Technical College in Linz/Austria, respectively.